What is claimed is:

1. An array substrate for an in-plane switching liquid crystal display device, comprising:

a gate line on a substrate;

a data line crossing the gate line to define a pixel region;

a semiconductor layer including an active area and a source area, wherein the active area overlaps the gate line and the source area overlaps the data line;

a drain electrode connected to the semiconductor layer;

a first capacitor electrode in the pixel region and connected to the drain electrode;

a pixel electrode connected to the first capacitor electrode and substantially in parallel to the data line;

a common line substantially parallel to the gate line;

a second capacitor electrode connected to the common line and overlapping the first capacitor electrode; and

a common electrode connected to the common line and alternatively arranged with the pixel electrode,

wherein the source area of the semiconductor layer, the drain electrode, the first capacitor electrode and the pixel electrode include doped polycrystalline silicon.

2. The array substrate of claim 1, wherein the semiconductor layer, the drain electrode, the first capacitor electrode and the pixel electrode are formed to be substantially integrated.

3. The array substrate of claim 1, further comprising a gate insulating layer under the gate line and the common line

4. The array substrate of claim 3, wherein the first and second capacitor electrodes form a storage capacitor having the gate insulating layer interposed therebetween.

5. The array substrate of claim 1, further comprising an inter insulating layer covering a thin film transistor, the thin film transistor including the semiconductor layer, a gate electrode, a source electrode and the drain electrode.

6. The array substrate of claim 5, wherein the inter insulating layer includes a source contact hole to expose the source area of the semiconductor layer, and the source electrode being connected to the semiconductor layer via the source contact hole.

7. The array substrate of claim 1, wherein the semiconductor layer is patterned using dry etching.

8. An array substrate for an in-plane switching liquid crystal display device, comprising:

a gate line on a substrate;

a data line crossing the gate line to define a pixel region;

a semiconductor layer including an active area and a source area, wherein the active area overlaps the gate line and the source area overlaps the data line;

a drain electrode connected to the semiconductor layer;

a first capacitor electrode in the pixel region and connected to the drain electrode;

a pixel electrode connected to the first capacitor electrode and substantially in parallel to the data line;

a first common line substantially parallel to the gate line;

a second capacitor electrode connected to the first common line and overlapping the first capacitor electrode;

an auxiliary capacitor electrode covering and connected to the second capacitor electrode;

a second common line covering and connected to the auxiliary capacitor electrode; and

a common electrode connected to the second common line and alternatively arranged with the pixel electrode,

wherein the source area of the semiconductor layer, the drain electrode, the first capacitor electrode and the pixel electrode include doped polycrystalline silicon.

9. The array substrate of claim 8, wherein the second common line and the common electrode are formed of a transparent conductive material.

10. The array substrate of claim 8, wherein the semiconductor layer, the drain electrode, the first capacitor electrode and the pixel electrode are formed as a single unit.

11. The array substrate of claim 8, further comprising a gate insulating layer under the gate line, the gate electrode, the first common line and the second capacitor electrode.

12. The array substrate of claim 11, wherein the first and second capacitor electrodes form a storage capacitor with the gate insulating layer interposed therebetween.

13. The array substrate of claim 11, further comprising an inter insulating layer covering a thin film transistor, the thin film transistor including the semiconductor layer, a gate electrode, a source electrode and the drain electrode.

14. The array substrate of claim 13, wherein the inter insulating layer includes a source contact hole to expose the source area of the semiconductor layer and a first contact hole to expose the second capacitor electrode, wherein the source electrode is connected to the semiconductor layer through the source contact hole and the auxiliary capacitor electrode is connected to the second capacitor electrode through the first contact hole.

15. The array substrate of claim 14, further comprising a passivation layer between the auxiliary capacitor electrode and the second common line.

16. The array substrate of claim 15, wherein the passivation layer includes a second contact hole to expose the auxiliary capacitor electrode, the second common line being connected to the auxiliary capacitor electrode through the second contact hole.

17. A method of fabricating an array substrate for an in-plane switching liquid crystal display device, comprising:

forming a semiconductor layer, a drain electrode, a first capacitor electrode and a pixel electrode on a substrate using polycrystalline silicon, the semiconductor layer including an active area and a source area;

forming a gate insulating layer, a gate line, a second capacitor electrode, a common line and a common electrode, wherein forming a gate insulating layer, a gate line, a second

capacitor electrode, a common line and a common electrode include forming a first insulating layer and a first metal layer on the substrate including the semiconductor layer, the drain electrode, the first capacitor electrode and the pixel electrode;

patterning the first insulating layer and the first metal layer, wherein the gate line overlaps the active area of the semiconductor layer, the second capacitor electrode covers the first capacitor electrode, and the common electrode extends from the common line;

forming an inter insulating layer to cover the gate line, the second capacitor electrode, the common line, and the common electrode by forming a second insulating layer and patterning the second insulating layer, the inter insulating layer having a source contact hole to expose the source area; and

forming a data line on the inter insulating layer, wherein forming a data line includes forming and patterning a second metal layer, the data line being connected to the source area through the source contact hole.

18. The method of claim 17, wherein the source area of the semiconductor layer, the drain electrode, the first capacitor electrode and the pixel electrode include doped polycrystalline silicon.

19. The method of claim 18, wherein the source area of the semiconductor layer, the drain electrode, the first capacitor electrode and the pixel electrode are one of n-type and p-type.

20. The method of claim 17, wherein forming the semiconductor layer, the drain electrode, the first capacitor electrode and the pixel electrode includes masking the active

area of the semiconductor layer and doping the source area of the semiconductor layer, the drain electrode, the first capacitor electrode and the pixel electrode.

21. An array substrate for an in-plane switching liquid crystal display device, comprising:

a gate line on a substrate in a first direction and including a gate electrode;

a data line in a second direction including a source electrode and crossing the gate line to define a pixel region;

a first capacitor electrode in the pixel region;

a common line of the second direction;

a common electrode extending from the common line;

a drain electrode spaced apart from the source electrode;

a second capacitor electrode overlapping the first capacitor electrode;

a pixel electrode alternatively arranged with the common electrode; and

a semiconductor layer covering the gate electrode and overlapping the source electrode, the semiconductor layer including an active layer and an ohmic contact layer,

wherein the ohmic contact layer, the drain electrode, the second capacitor electrode and the pixel electrode include doped amorphous silicon permitting light-transmission.

22. The array substrate of claim 21, wherein the drain electrode, the first capacitor electrode and the pixel electrode are formed as a substantially integrated body.

23. An array substrate for an in-plane switching liquid crystal display device, comprising:

a gate line of a first direction;

a data line of a second direction, wherein the data line crosses the gate line to define a pixel region;

a thin film transistor arranged at a crossing of the gate and data lines;

a pixel electrode of the second direction connected to the thin film transistor, the pixel electrode including doped semiconductor material permitting light-transmission; and

a common electrode of the second direction alternatively arranged with the pixel electrode.